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HAYES SOLOWAY P.C. 3450 E. SUNRISE DRIVE, SUITE 140 TUCSON, AZ 85718			GEBREYESUS, YOSEF	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/599,235	TAGO, MASAMOTO	
	<b>Examiner</b>	<b>Art Unit</b>	
	YOSEF GEBREYESUS	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 03 April 2009.  
 2a) This action is **FINAL**.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 25-38 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 25-38 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 22 September 2006 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)          | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ .                                    |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____.   | 6) <input type="checkbox"/> Other: _____ .                        |

## DETAILED ACTION

### ***Priority***

Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Japan on 03/25/2004. It is noted, however, that applicant has not filed a certified copy of the 2004-089199 application as required by 35 U.S.C. 119(b).

### ***Drawings***

Figures 9 and 10 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: On page 27, paragraph [0049], line 22, "chip 8". Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of

an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Specification***

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required:

Even though the drawing shows the claimed invention the following limitations are not disclosed in the specification.

Claim 31 recites the limitation "first conducting member" in lines 7, 12 and 14 and "second conducting member" in lines 9 and 13.

The disclosure is objected to because of the following informalities: On page 22, paragraph [0042] line 24 "2c" appears to be "2b".

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Appropriate correction is required.

***Claim Objections***

Claim 38 is objected to because of the following informalities: Claim 38 recites the limitation “wherein said electrical connector at least one bump”, it appears to be “wherein said electrical connector is at least one bump”. It is suggested to change “wherein said electrical connector at least one bump” to “wherein said electrical connector is at least one bump” for clarity. Appropriate correction is required.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 25-26,29,30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chikawa et al. (US 6,836,002) in view of Dotta et al. (US 2004/0080040).

Regarding claim 25, Figure 1(b) of Chikawa et al. discloses a stacked-chip semiconductor device 1 comprising: an interposer substrate 2; and a plurality of semiconductor chips 3 and 4 overlaid two tiers deep and mounted on said interposer chip 2, where in at least one of said semiconductor chips has a thick film wiring 6, and a voltage is fed from said interposer substrate 2 by way of thick-film wiring 6 to a circuit surface (col. 3 lines36-37) of another semiconductor chip 4 that is disposed above said semiconductor chip 3. Chikawa et al. does not expressly teach the electrical

connection is at least one voltage selected from power supply and voltage and ground. However, Figure 1a, 1b and 9 Dotta et al. teaches stacked-chip semiconductor device 40, wherein the first conducting member 8 that feeds a power supply 8a and ground 8b (paragraph [0040]) to the circuit surface of said first semiconductor chip 1a, and at least one voltage selected from power supply voltage and ground is fed from said interposer substrate 30 to the circuit surface of said first semiconductor chip 1a. Therefore it would have been obvious to one ordinary skill in the art at the time the invention was made to modify the invention of Chikawa et al. by teachings of Dotta et al. to connect the semiconductor chips with power supply voltage and ground in order to operate the semiconductor devices.

Regarding claim 26, Figure 1(b) of Chikawa discloses all the claimed invention as applied to claim 25 above. Figure 1(b) of Chikawa discloses a plurality of semiconductor chips being composed of: a first semiconductor chip 3 that has a circuit surface on upper surface (col. 4 line 66-67) and said thick film wiring; and second semiconductor chip 4 that is disposed above said first semiconductor chip 3 bonding wires for electrically connecting said interposer substrate 2 and thick-film wiring 6 and bonding wires 7 for electrical connecting (col. 3 lines 58-61). Chikawa failed to disclose a plurality of bumps for providing electrical connection and a plurality of through wires on a second semiconductor chip 4 and at least one voltage selected from power supply voltage and ground is fed through. However, in the same field of endeavor, Figure (10 and13) of Dotta et al. discloses a plurality of bumps 310 between the semiconductor devices 301a and 301b and plurality of through wires 306 (paragraph [0009]) to

establish electrical connection between the interposer substrate 30 and the semiconductor chip 1b. Dotta et al. also teaches in a semiconductor device the through electrode has multiple power-supply though electrodes, grounding and signal routing (paragraph [0400]). In view of such teaching, it would have been obvious to modify the invention of Chikawa et al. as taught by Dotta et al. to form semiconductor chips with a plurality of through-wires on the top semiconductor chip by eliminating the need of bonding wires on the top chip for the purpose reducing the chip size package. Also it would have been obvious to modify the invention of Chikawa et al. as taught by Dotta et al to form a bump between the semiconductor chips 301a and 301b for the purpose of reducing power loss.

Regarding claim 29 Figure 1(b) of Chikawa discloses all the claimed inventions as applied to claim 25. Chikawa teaches using a thick film wiring and an electrode pad formed together at the same height in order to stack chips. Chikawa does not teach using a separate bump as mentioned above. Also Chikawa lacks to teach the thickness of said thick-film wiring is the same as the height of said plurality of bumps. However, Figure 2 and 9 of Dotta et al. teaches using a bump 25 as connecting terminal between interposer 30 and first chip 1a, and between first chip 1a and second chip 1b. Therefore it would have been obvious to one ordinary skill in the art to form a bump and a thick film wiring with the same height. Moreover, there is no evidence that indicates the height of the bump and the thick-film wiring be the same is critical and it has been held that it is not inventive to discover the optimum workable height of a result-effective variable with given prior art conditions by routine experimentation. See MPEP 2144.05

Note that the specification contains no disclosure the critical nature the claimed height of any unexpected results there from.

Regarding claim 30, the limitation "are formed by plating" is merely product-by-process limitation that does not structurally distinguish the claimed invention over the prior art. The patentability of a product does not depend on its method of production. If the product in the product by process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process. *In re Thrope*, 227 USPQ 964, 966

Claim 27 is rejected under 35 U.S.C 103(a) as being unpatentable over Chikawa et al. US (6,836,002) in view of Dotta et al. (US 2004/0080040) as applied to claim 25 above, and further in view of Saeki (US 7,132,752).

Regarding claim 27, Figure 1(b) of Chikawa et al. discloses a plurality of semiconductor chips 3 and 4 being composed of; a first semiconductor chip 3 that has a circuit surface on upper surface and thick-film wiring 6; and a second semiconductor chip 4 that is disposed above said first semiconductor chip 3, comprising; bonding wires 7 for electrically connecting said interposer substrate 2 and said thick film wiring 6. Chikawa does not expressly teach the following limitations:

a plurality bumps for providing an electrical connection between said second semiconductor chip 4 and said thick-film wiring 6.

other bonding wires for providing an electrical connection between said interposer substrate 2 and said second semiconductor chip 4.

However, in the same field of endeavor Figure 13 of Dotta et al. teaches a bump (connecting terminals) 310 for providing electrical connection between said second semiconductor chip 301b and thick film wiring 303 (paragraph [0009]). Moreover, Figure 2B of Saeki teaches other bonding wires 148 for providing an electrical connection between said interposer substrate 100 and said second semiconductor chip 110-2, electrical signals are transmitted (col. 12 lines 5-7) between the circuit surface (top surface) of said second semiconductor chip 110-2 and said interposer substrate 100 (substrate) (col. 8 line 28-29) by way of said plurality through-wires 106 and said other bonding wires 148. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Chikawa as taught by Dotta et al. and Saeki to form bumps between the upper and lower chip for electrical connection in order to avoid using external wiring for the purpose of reducing chip packaging size.

Claim 28 is rejected under 35 U.S.C 103(a) as being unpatentable over Chikawa et al. US (6,836,002) in view of Dotta as applied to claim 25 above, and in further view of Smola et al. (US 6,388,320).

Regarding claim 28, Figure 1b of Chikawa et al. discloses a stacked-chip semiconductor 3 and 4 electrical connection is formed from the interposer 2 by way of thick-film wiring 6 to the another semiconductor chip 4. Chikawa does not teach a spacer is formed with through wires disposed between the semiconductor chips 3 and 4. However, in the same field of endeavor Figure 2 of Smola teaches a spacer 7 formed

with through-wires 17 is disposed between said semiconductor chip 1 and 10 for electrical connection (col. 4 lines 36-40). Therefore, in view of such teaching it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Chikawa with the teachings of Smola et al. to use a spacer with through-wiring between semiconductor chips for the purpose of low power dissipation, less signal delay and for stacked-chip structural support.

Claims 31 and 38 are rejected under 35 U.S.C 103(a) as being unpatentable over Chikawa et al. US (6,836,002) in view of Dotta et al. (US 2004/080040) and Sugizaki (US 2002/0041027).

Regarding claim 31, Figure 1(b) of Chikawa et al. discloses an interposer substrate 2, first semiconductor chip 3, a second semiconductor chip 4, first and second conducting member 7 for electrical connection (col.5 lines 55-60), an electrical connector (second electrode pad) 6b electrically connecting the first semiconductor chip 3 and the second semiconductor chip 4 (col. 5 lines 55-61).

Chikawa et al. failed to disclose the following limitations: the first semiconductor chip 2 has a plurality of through-wires; the second semiconductor chip 2 has a circuit on lower surface, a first conducting member feeds at least one voltage selected from power supply and ground to a circuit surface of said first semiconductor chip, a second conducting member that feeds at least one voltage and ground to said circuit surface of said second semiconductor chip, wherein said first conductive member and said second conductive member are mutually independent routes.

However, in the same field of endeavor Figure 1(a) and 9 of Dotta et al. discloses a stacked-semiconductor device 40 comprising: an interposer substrate 30, a first semiconductor chip 1a that is disposed above said interposer substrate 30 and that has a plurality of through-wires 18; a second semiconductor chip 1b that is disposed above said first semiconductor chip 1a; a first conduction member 8a that feeds at least one voltage selected from power supply voltage and ground to a circuit surface (paragraph [0007]); and a second conducting member 8a that feeds at least voltage selected from power supply voltage 8a and ground 8b (paragraph [0040]) to a circuit surface of said first semiconductor chip 1a; and a second conducting member that feeds at least one voltage selected from power supply voltage to said circuit surface of second semiconductor chip 1b, where in said first conductive member and said second conductive member are mutually independent routes (paragraph [0093]). Moreover, Figure 17 of Sugizaki teaches a stacked-semiconductor device comprising a second semiconductor chip 1-2 disposed on top of first semiconductor device 1-1, where the second semiconductor chip 1-2 has circuit surface (element formation surface) 2 (paragraph [0077]) on the lower surface. Therefore In view of such teaching it would have been obvious to one ordinary skill in the art at the time the invention was made to modify the invention of Chikawa et al. with teachings of Dotta et al. and Sugizaki to form a first semiconductor chip with a plurality of through wires for a purpose of avoiding using external wiring which helps to increase the chip speed, to use the lower surface of the second semiconductor chip as a circuit surface for ease of connection, to form mutually independent first and second conductive members for first chip and second

chip respectively for the purpose of stacking semiconductor chips which uses different power or voltage.

Regarding claim 38, figure 1b of Chikawa et al. discloses wherein said electrical connector (electrode pad) 6b is at least one bump (pad) 6b (col. 5 lines 38-41).

Claims 32, 34, 35-37 are rejected under 35 U.S.C 103(a) as being unpatentable over Chikawa et al. US (6,836,002), Sugizaki (US 2002/0041027) as applied to claim 31 above, and in further view of Dotta et al. (US 2004/080040).

Regarding claim 32, Chikawa et al. and Sugizaki disclose all the claimed inventions as applied to claim 31. Chikawa and Sugizaki lack to disclose the second semiconductor chip 4 has a plurality of through-wires disposed on the said first semiconductor chip 3. However, Figure 1(a) and 9 of Dotta et al. discloses a stacked-chip semiconductor device 40, wherein the second conducting member 8c that feeds a power supply and ground to the circuit surface of said second semiconductor chip has a plurality of through-wires 18 disposed on said first semiconductor chip 1a, and at least one voltage selected from power supply voltage and ground (paragraph [0040]) is fed from said interposer substrate 30 to the circuit surface of said second semiconductor chip by way of said plurality of through-wires 8a and 8c (paragraph [0093]). Therefore it would have been obvious to one ordinary skill in the art at the time the invention was made to modify the teaching of Chikawa et al and Sugizaki with the teachings of Dotta et al to form a second semiconductor chip 4 with a plurality of through wires for a

voltage and ground that is fed from the interposer for the purpose of forming compact size chips and to reduce voltage drops caused by external wirings.

Regarding claim 34, Chikawa et al. and Sugizaki disclose all the claimed inventions as applied to claim 31. Chikawa teaches the semiconductor chips 3 and 4 are electrically connected with the package external lead 2a. Chikawa et al. and Sugizaki failed to disclose the first conducting member 7 feeds power supply voltage and ground to a circuit surface of said first semiconductor chip 3. However, Figure 9 and 13 of Dotta et al. discloses the stacked-chip semiconductor device 300, wherein the first conducting member that feeds a power supply and ground to the circuit (paragraph [0040]) surface of said first semiconductor chip 301a, and at least one voltage selected from power supply voltage and ground is fed from said interposer substrate 30 to the circuit surface of said first semiconductor chip by way of thick film wiring 303. Therefore it would have been obvious to one ordinary skill in the art at the time the invention was made to modify the teachings of Chikawa et al. and Sugizaki with the teachings of Dotta et al. to use the first conducting member to feed power supply voltage and ground to semiconductor chip for the purpose of operating semiconductor devices.

Regarding claim 35, Chikawa et al. and Sugizaki disclose all the claimed inventions as applied to claim 31. Chikawa et al. and Sugizaki do not teach a plurality of bumps for electrically connecting and plurality of through-wires of said first semiconductor chip. However, Figure 2 and 13 of Dotta et al. discloses the stacked-chip semiconductor device, comprising a plurality of first bumps 25 for connecting the plurality of through-wires 306 of said first semiconductor chip 301a and said interposer

substrate 30; and a plurality of second bumps 25 for electrically connecting the plurality of through-wires 306 of said first semiconductor chip 1a and said second semiconductor chip 1b (paragraph [0009]). Therefore it would have been obvious to one ordinary skill in the art at time the invention was made to modify the teachings of Chikawa et al. and Sugizaki with the teachings of Dotta et al. form a semiconductor devices with a plurality of bumps and through wires by forming bumps to connect semiconductor chips for the purpose be reducing power loss and to form a semiconductor device with through wires for the purpose of fast signal response and forming small size package chips.

Regarding claim 36 and 37 Chikawa and Sugizaki disclose all the claimed inventions as applied to claim 31. Chikawa teaches using a thick film wiring and an electrode pad formed together at the same height in order to stack chips. Chikawa and Sugizaki do not teach using a separate bump as mentioned above. Also Chikawa and Sugizaki lack to teach the thickness of said thick-film wiring is the same as the height of said plurality of bumps. However, Figure 2 and 9 of Dotta et al. teaches using a bump 25 as connecting terminal between interposer 30 and first chip 1a, and between first chip 1a and second chip 1b. Therefore it would have been obvious to one ordinary skill in the art to form a bump and a thick film wiring with the same height. Moreover, there is no evidence that indicates the height of the bump and the thick-film wiring be the same is critical and it has been held that it is not inventive to discover the optimum workable height of a result-effective variable with given prior art conditions by routine experimentation. See MPEP 2144.05 Note that the specification contains no disclosure the critical nature the claimed height of any unexpected results there from.

Claim 33 is rejected under 35 U.S.C 103(a) as being unpatentable over Chikawa et al. US (6,836,002), Sugizaki (US 2002/0041027) as applied to claim 31 above, and in view Dotta et al. (US 2004/0080040), and further in view of Smola et al. (US 6,388,320).

Regarding claim 33, Chikawa et al. and Sugizaki teaches all the features previously outlined. Chikawa and Sugizaki failed to disclose a spacer that has plurality of through-wires is disposed between first and second chips and power is supplied from the interposer by way of through-wires of said spacer to the circuit surface of second semiconductor chip. However, in the same field of endeavor Figure 9 and 13 of Dotta et al. discloses a stacked-chip semiconductor device 300, where in a circuit layer (wiring layer with insulating film) 303 and 308 that has a plurality of through-wires 306 is disposed between said first semiconductor chip 301a and second semiconductor chip 301b, and at least one voltage selected from power supply voltage and ground (paragraph [0040]) is fed from said interposer 30 (paragraph [0046]) by way of though wires 8 of said first semiconductor chip 301a and the through-wires (309 and 310) of said spacer 303 to the circuit surface of second semiconductor chip 301b. Moreover, Figure 2 of Smola teaches a spacer 7 formed with through-wires 17 is disposed between said semiconductor chip 1 and 10 for electrical connection (col. 4 lines 36-40). Therefore, in view of such teaching it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Chikawa and Sugizaki with the teachings of Dotta et al. and Smola to use a spacer with through-

wiring between semiconductor chips for the purpose of low power dissipation, less signal delay and for stacked-chip structural support.

***Response to Arguments***

Applicant's amendment filed on April 3<sup>rd</sup>, 2009 and forwarded to examiner on May 29<sup>th</sup>, 2009, overcame the US 112, 2<sup>nd</sup> rejection. The US 112, 2<sup>nd</sup> rejection has been withdrawn. The Applicant's argument to drawings (Figure 8) is persuasive. The objection to drawings about the thickness of thick film wiring is withdrawn.

Claims 25, 31 and 33 as amended by the amendment and claims 26-30, 32 and 34-37 as previously cited are currently in the application, presently newly added claim 38.

Applicant's arguments with respect to claims 25-30 have been fully considered but are not persuasive.

Applicant's arguments with respect to claim 25-37 have been fully considered but they are not persuasive in view of the new ground(s) of rejection. The examiner would like to emphasize the new ground(s) of rejection is established because Applicant has added the limitation "an electrical connector electrically connecting the first semiconductor chip, wherein a current path from the first conducting member to the second conducting member includes the electrical connector " in claim 31 and "wherein said electrical connector at least one bump" in new claim 38.

Regarding claim 25, Applicant's argues that Chikawa does not teach the power supply voltage and ground is fed by "way of thick film wiring". However, the examiner

respectfully disagrees. Examiner would like to clarify that Chikawa indeed teaches electrical connection is established by way of the rewiring layer (col. 3 lines 29-44). The rewiring layer is considered the same as Applicant's claimed "thick film wiring". Even though Chikawa does not use the claimed language power supply voltage and ground, the examiner is required to use broadest reasonable interpretation to examine the claims (MPEP 2111). As a result electrical connection is considered as power (voltage or current) and ground connection.

Next, Applicant argues that Chikawa's rewiring layer is overwhelmingly thinner than that of the interposer and the thickness of the package should be suppressed. Dotta discloses an increase in area of through electrode is required. The requirements for the rewiring layer of Chikawa and through electrode of Dotta are mutually exclusive and could not be combined. However, examiner respectfully disagrees. Dotta discloses the through electrode 8a and the semiconductor chips 1a and 1b are formed to achieve compactness and slimness (paragraph [0100]). Both Chikawa and Dotta disclose reducing a device size. Hence, the rewiring layer of Chikawa and the thorough electrode of Dotta are not mutually exclusive and can be combined.

Regarding claim 31, Applicant argues that Dotta fails to disclose a current path between the first and second conducting members. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., a current path between the first conducting second conducting member) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are

not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). However, Dotta discloses the power supply terminal and ground terminal conduct electric current (paragraph [0040] and [0101]). Further, Applicant's argues that Sugizaki fails to disclose the current path and an independent route. Examiner would like to clarify that since Dotta teaches the current path and an independent route (paragraph [0093]); Sugizaki is not used for a teaching of a current path and an independent route. As mentioned in the office action the teaching's of Sugizaki is used for the claimed limitation of the second semiconductor chip has a circuit surface on a lower surface.

For the reasons mentioned above the Applicant's arguments is not found persuasive.

### ***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to YOSEF GEBREYESUS whose telephone number is (571)270-5765. The examiner can normally be reached on Monday through Thursday 7:30 to 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne A. Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Lynne A. Gurley/  
Supervisory Patent Examiner, Art  
Unit 2811

Yosef Gebreyesus  
07/17/2009

Art Unit: 2811

/Y. G./

Examiner, Art Unit 2811